WHAT IS CLAIMED IS:

1. A magnetic memory comprising:

a plurality of digit lines;

a plurality of bit lines, wherein the digit lines and the bit lines intersect each other at an oblique angle; and

magnetic tunnel junctions (MTJs) between the bit lines and the digit lines.

2. The magnetic memory of claim 1, wherein the digit lines and the bit lines intersect each other at an oblique angle of between 15° to 75°.

3. The magnetic memory of claim 1, wherein the MTJs are directly connected to the bit lines, and are spaced apart from the digit lines.

4. The magnetic memory of claim 1, further comprising a plurality of cell transistors, wherein the cell transistors are arrayed along a row direction and a column direction, wherein the cell transistors comprise a gate electrode, a source region and a drain region, and wherein the gate electrodes of the cell transistors are connected to each other through a plurality of word lines.

5. The magnetic memory of claim 4, wherein the digit lines are parallel to the word lines, and the bit lines intersect the word lines at an oblique angle.

6. The magnetic memory of claim 5, wherein the bit lines diagonally connect the drain regions of the cell transistors to each other.

7. The magnetic memory of claim 5, wherein the bit lines zigzag to connect the drain regions of the cell transistors to each other.

8. The magnetic memory of claim 4, wherein the bit lines intersect the word lines perpendicularly, and the digit lines intersect the word lines at an oblique angle.

9. The magnetic memory of claim 8, wherein the digit lines diagonally intersect the cell transistors.

10. The magnetic memory of claim 8, wherein the digit lines intersect the cell transistors in a zigzag pattern.

11. The magnetic memory of claim 1, wherein the MTJs comprise a pinning layer, a fixed layer, an insulating layer and a free layer.

12. The magnetic memory of claim 11, wherein the fixed layer comprises a lower ferromagnetic film, a ruthenium film and an upper ferromagnetic film.

13. The magnetic memory of claim 1, wherein the MTJs have a rectangular shape.

14. The magnetic memory of claim 1, wherein the MTJs have a parallelogram shape.

15. The magnetic memory of claim 1, wherein the MTJs have a parallelogram shape with rounded corner portions.

16. A fabricating method of a magnetic memory, the method comprising:

forming a plurality of digit lines;

forming a plurality of bit lines, wherein the bit lines intersect the digit lines at an oblique angle;

forming a plurality of Magnetic Tunnel Junctions (MTJs) that are between the bit lines and the digit lines.

17. The method of claim 16, further comprising forming an upper interlayer insulating film on the digit lines, and wherein the Magnetic Tunnel Junctions (MTJs) are formed on the upper interlayer insulating film.

18. The method of claim 17, further comprising the steps of:

forming cell transistors that are arrayed along a row direction and a column direction prior to forming the digit lines.

19. The method of claim 18, wherein forming cell transistors that are arrayed along a row direction and a column direction comprises:

forming device isolation regions in a semiconductor substrate to define active regions;

forming word lines that intersect the active regions; and

forming drain regions and source regions in the active regions between the word lines.

20. The method of claim 19, further comprising:

forming a lower interlayer insulating film on the cell transistors prior to forming the digit lines; and

forming wirings passing through the upper interlayer insulating film and the lower interlayer insulating film to connect the drain regions of the cell transistors to the MTJs.

21. The method of claim 20, wherein the bit lines are connected to the drain regions through the vertical wirings and intersect the word lines at an oblique angle.

22. The method of claim 20, wherein the bit lines intersect the word lines in a zigzag pattern.

23. The method of claim 20, wherein the bit lines diagonally connect the drain regions of the cell transistors to one another.

24. The method of claim 18, wherein forming a lower interlayer insulating film on the cell transistors prior to forming the digit lines comprises of the steps of:

forming a first lower interlayer insulating film on an entire surface that includes the cell transistors;

forming contact plugs that penetrate the first lower interlayer insulating film and connect to the drain regions and the source regions;

forming first metallic patterns on the contact plugs and the first lower interlayer insulating film;

forming a second lower interlayer insulating film on the first metallic patterns; and

forming via plugs that penetrate the second lower interlayer insulating film and connect to the first metallic patterns,

wherein the first metallic patterns form a source line connecting the source regions by the contact plugs, and form pads connecting the via plugs with the drain regions by the contact plugs.

25. The method of claim 19, wherein the digit lines intersect the word lines at an oblique angle.

26. The method of claim 19, wherein the digit lines diagonally pass over the cell transistors that are arrayed in row and column directions.

27. The method of claim 16, wherein the digit lines zigzag.

28. The method of claim 16, wherein the MTJs are formed with a parallelogram shape with rounded corner portions.